Instruction Manual

Tektronix

TMS 163
i960 Jx Microprocessor Support

070-9817-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 163 i960 Jx microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 163 i960 Jx support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names must be replaced with 960JX. This is the name of the microprocessor in field selections and file names you must use to operate the i960 Jx support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 102/136-channel or a 96-channel module.
- 960JX refers to all supported variations of the i960 Jx microprocessor unless otherwise noted.
- An asterisk (*) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics and tasks:

- A description of the TMS 163 microprocessor support package
- Logic analyzer software compatibility
- Your system under test requirements
- Support restrictions
- How to configure the probe adapter
- How to connect to the system under test (SUT)
- How to apply power to and remove power from the probe adapter

Support Description

The TMS 163 microprocessor support package disassembles data from systems that are based on the Intel i960 Jx microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 163 microprocessor support.

Table 1–1 shows which microprocessors, packages, and clock rates the TMS 163 product supports.

Table 1–1: Supported microprocessors

Microprocessor	Package*	Clock rate
i960 JA	PGA, QFP	16, 25, & 33 MHz
i960 JD	PGA, QFP	16 & 25 MHz
i960 JF	PGA, QFP	16, 25, & 33 MHz

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *i960 Jx Microprocessor User's Manual*, Intel, 1994.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the i960 Jx support, the Tektronix logic analyzer must be equipped with either a 102/136-channel module, or a 96-channel module at a minimum. The module must be equipped with enough probes to acquire channel and clock data from signals in your i960 Jx-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other i960 Jx support requirements and restrictions.

System Clock Rate. The TMS 163 support can acquire data from the i960 Jx microprocessor at speeds of up to 33 MHz for 960 JA/JF[1] and 25 MHz for 960 JD; it has been tested to 33 MHz for 960 JF microprocessor.

Disabling the Instruction Cache, Data Cache, and Vector Cache. To disassemble acquired data, you must disable the internal Instruction cache, the internal Data cache. Disabling the caches makes all instruction prefetches visible on the bus so they can be acquired and disassembled.

Vector caching has to be disabled so that microprocessor fetches the interrupt vector entries from external RAM and not from internal RAM. This will reflect the vector reads to external bus.

1 **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

Configuring the Probe Adapter

If your system under test (SUT) has a +3 V i960 Jx microprocessor or you do not want the SUT to provide power to the probe adapter when the probe adapter is in an SUT with a +5 V microprocessor, you can use an alternate power source. If you use an alternate power source, you need to place the Power Source jumper on pins 1 and 2.

If your SUT has a +5 V i960 Jx microprocessor, and the probe adapter will be powered from the SUT, you need to place the Power Source jumper on pins 2 and 3.

For more information on using an alternate power source, refer to *Applying and Removing Power Using an Alternate Source* in this chapter.

Figure 1–1 shows the location of the Power Source jumper.

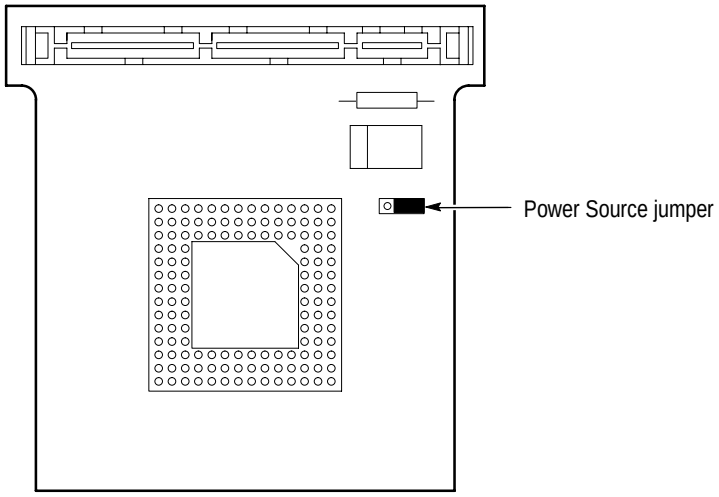


Figure 1–1: Power Source jumper location

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. The probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

Probe Adapter with a High-Density Probe

To connect the logic analyzer to an SUT using the PGA probe adapter and a high-density probe, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the low-profile probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and low-profile probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch the black foam on the underside of the probe adapter to discharge stored static electricity from the probe adapter.
3. Remove the microprocessor from the SUT.
4. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

5. Place the microprocessor into the probe adapter as shown in Figure 1–2.

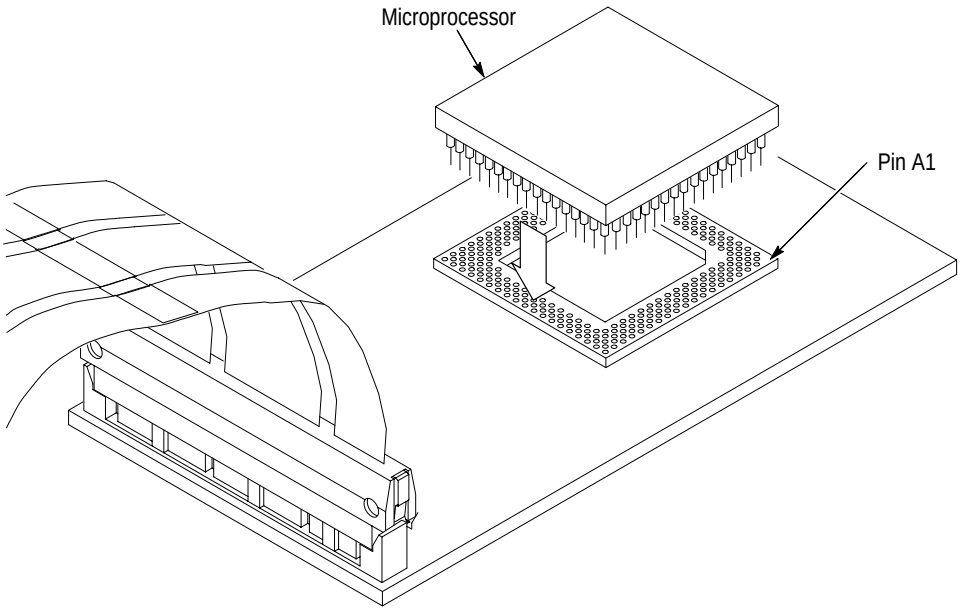


Figure 1–2: Placing a microprocessor into the probe adapter

6. Remove the black foam from the underside of the probe adapter.

7. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the SUT.

8. Place the probe adapter onto the SUT as shown in Figure 1–3.

NOTE*. You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind this might increase loading, which can reduce the electrical performance of the probe adapter.*

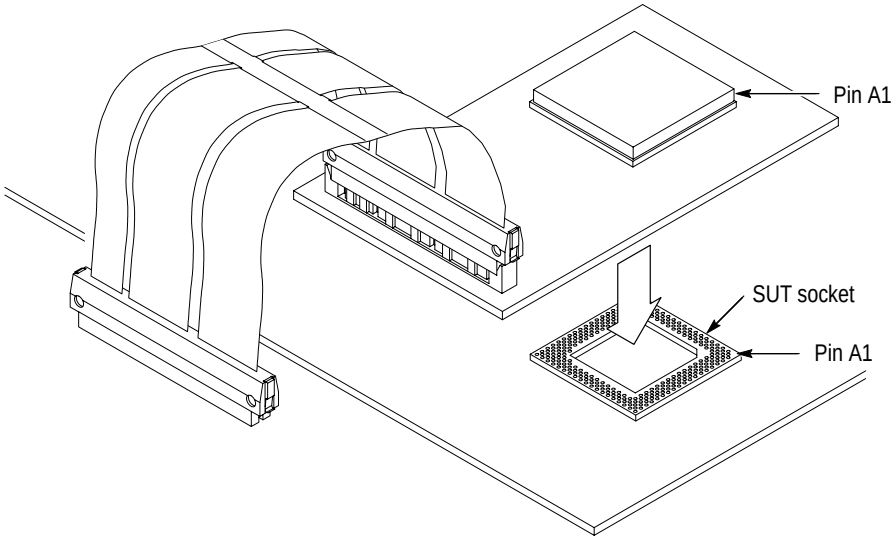


Figure 1–3: Placing a PGA probe adapter onto the SUT

9. Connect the channel and clock probes to the high-density probe as shown in Figure 1–4. Match the channel groups and numbers on the probe labels to the corresponding pins on the high-density probe. Match the ground pins on the probes to the corresponding pins on the probe adapter.

Since the data bus is multiplexed with the address bus, acquisition probes D3:7-0, D2:7-0, D1:7-0, and D0:7-4, do not have to be connected. Even if the probes are not connected, the Data channel group will still acquire data through the address bus. Since data is being acquired, these probes are not considered to be extra channels that you can use to connect to other signals in your SUT.

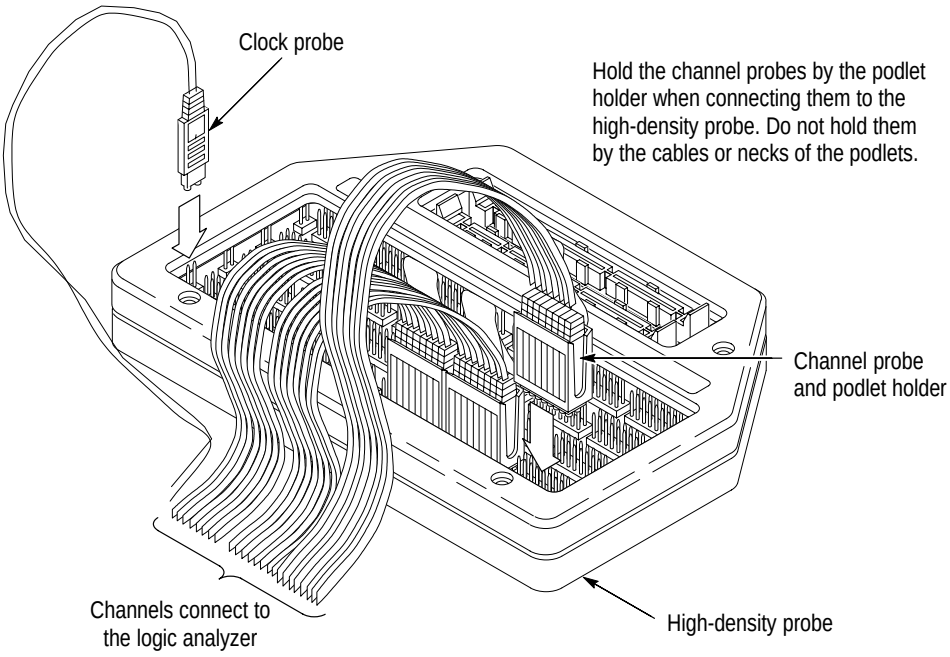


Figure 1–4: Connecting channel and clock probes to a high-density probe

10. Align pin 1 on the LO cable connector, the end on the narrowest cable strip of the cable, with pin 1 on the LO connector on the high-density probe. Connect the cable to the connector as shown in Figure 1–5.

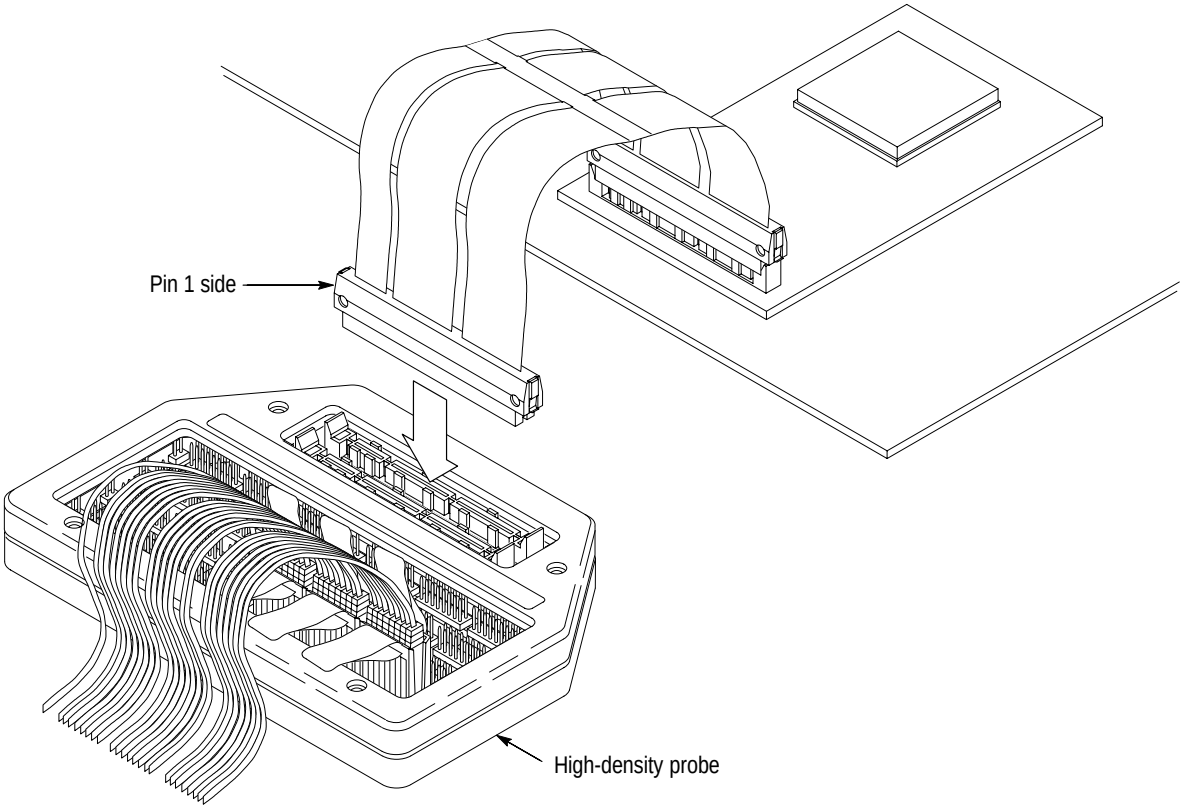


Figure 1–5: Connecting the cable to a high-density probe

With a PGA-to-QFP Converter Clip

To connect the logic analyzer to a SUT using the probe adapter, a PGA-to-QFP converter clip, and ahigh-density probe, follow these steps:

1. Line up the pin A1 indicator on the probe adapter board with the pin E1 indicator on the converter clip as shown in Figure 1–6.

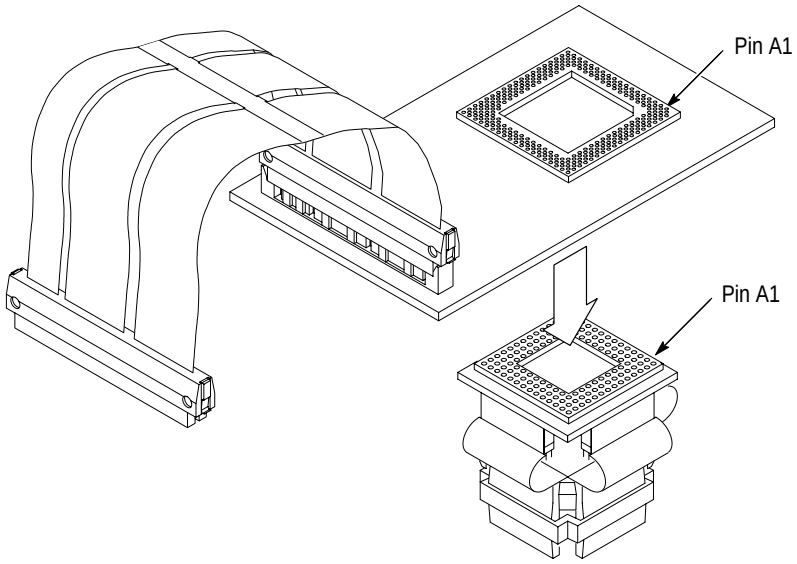


Figure 1–6: Placing the converter clip onto the probe adapter

2. Line up the pin A1 indicator on the probe adapter board with the pin E1 indicator on the SUT.

3. Place the probe adapter onto the SUT as shown in Figure 1–7.

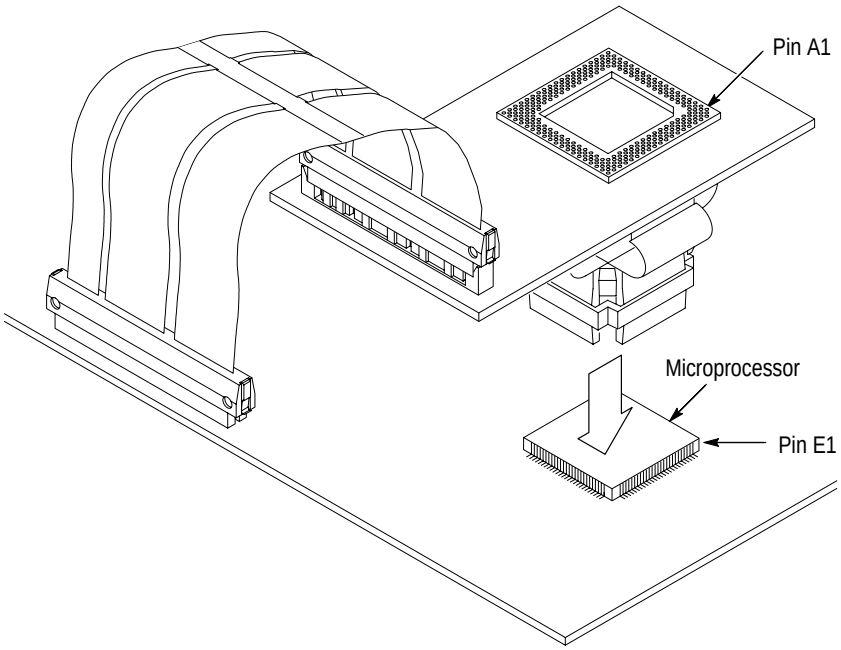


Figure 1–7: Placing the probe adapter onto the SUT

4. Press down on the probe adapter to secure the clip on the microprocessor.
5. Continue with steps 9 and 10 from the previous procedure.

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to i960 Jx signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

CAUTION. *Failure to place the SUT on a horizontal surface before connecting the test clip might permanently damage the pins on the microprocessor.*

3. Place the SUT on a horizontal static-free surface.
4. Use Table 1–2 to connect the channel probes to i960 Jx signal pins on the test clip or in the SUT.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

NOTE*. Since the microprocessor multiplexes the Address and Data buses, the D3:7-0, D2:7-0, D1:7-0 and D0:7-0 channel probes do not need to be connected. Although they are not connected, they are not considered to be extra channels. Do not use them to make connections to other signals in your SUT.*

Table 1–2: i960 Jx signal connections for channel probes

Section:channel	i960 Jx signal	Section:channel	i960 Jx signal
A3:7	AD31	D3:7	AD31
A3:6	AD30	D3:6	AD30
A3:5	AD29	D3:5	AD29
A3:4	AD28	D3:4	AD28
A3:3	AD27	D3:3	AD27
A3:2	AD26	D3:2	AD26
A3:1	AD25	D3:1	AD25
A3:0	AD24	D3:0	AD24
A2:7	AD23	D2:7	AD23
A2:6	AD22	D2:6	AD22
A2:5	AD21	D2:5	AD21
A2:4	AD20	D2:4	AD20
A2:3	AD19	D2:3	AD19
A2:2	AD18	D2:2	AD18
A2:1	AD17	D2:1	AD17
A2:0	AD16	D2:0	AD16
A1:7	AD15	D1:7	AD15
A1:6	AD14	D1:6	AD14
A1:5	AD13	D1:5	AD13
A1:4	AD12	D1:4	AD12
A1:3	AD11	D1:3	AD11
A1:2	AD10	D1:2	AD10
A1:1	AD9	D1:1	AD9
A1:0	AD8	D1:0	AD8
A0:7	AD7	D0:7	AD7
A0:6	AD6	D0:6	AD6
A0:5	AD5	D0:5	AD5
A0:4	AD4	D0:4	AD4
A0:3	A3	D0:3	AD3
A0:2	A2	D0:2	AD2
A0:1	GND	D0:1	AD1
A0:0	GND	D0:0	AD0
C3:7	CLKIN	C1:7	XINT7*
C3:6	BE3*	C1:6	XINT3*
C3:5	BE1*	C1:5	ALE

Table 1–2: i960 Jx signal connections for channel probes (cont.)

Section:channel	i960 Jx signal	Section:channel	i960 Jx signal
C3:4	W/R*	C1:4	BSTAT
C3:3	RESET*	C1:3	XINT6*
C3:2	BE2*	C1:2	XINT2*
C3:1	BE0*	C1:1	DT/R*
C3:0	WIDTH1	C1:0	FAIL*
C2:7	LOCK*	C0:7	XINT5*
C2:6	D/C*	C0:6	XINT1*
C2:5	BLAST*	C0:5	NMI*
C2:4	WIDTH0	C0:4	TDI
C2:3	HOLDA	C0:3	XINT4*
C2:2	RDYRCV*	C0:2	XINT0*
C2:1	DEN*	C0:1	HOLD
C2:0	ADS*	C0:0	TDO

Table 1–3 shows the clock probes and the i960 Jx signal to which they must connect for disassembly to be correct.

Table 1–3: i960 Jx signal connections for clock probes

Section:channel	i960 Jx signal
CK:1	BLAST*=
CK:0	CLKIN=

5. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the i960 Jx microprocessor in your SUT and attach the clip.

Applying and Removing Power

If your microprocessor system cannot supply power to the i960 Jx probe adapter or your system has a +3 V i960 Jx microprocessor (probe adapters need +5 V), you must use an alternate power source. A +5 V power supply is included with this support product.

The alternate power supply provides +5 volts to the i960 Jx probe adapter. The center connector of the power jack connects to Vcc.

To use the power supply, you need to position the Power Source jumper on pins 1 and 2.

To apply power to the i960 Jx probe adapter and SUT, follow these steps:

CAUTION. *Failure to use the +5 V power supply provided by Tektronix might permanently damage the probe adapter and i960 Jx microprocessor. Do not mistake another power supply that looks similar for the +5 V power supply.*

1. Connect the +5 V power supply to the jack on the probe adapter. Figure 1–8 shows the location of the jack on the adapter board.

CAUTION. *Failure to apply power to the probe adapter before applying power to your SUT might permanently damage the i960 Jx microprocessor and SUT.*

2. Plug the power supply for the probe adapter into an electrical outlet.
3. Power on the SUT.

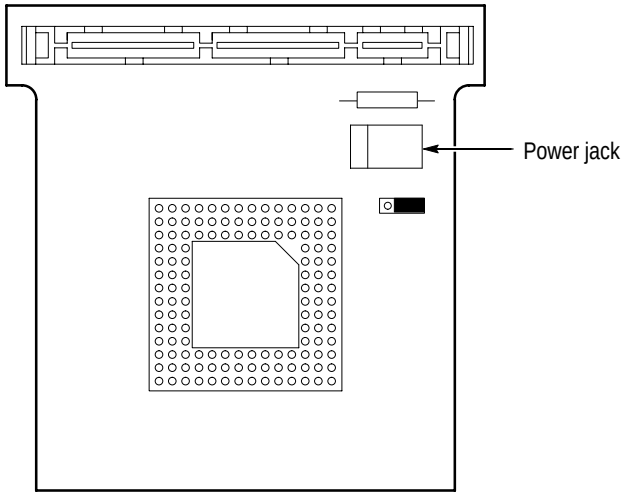


Figure 1–8: Location of the power jack

To remove power from the SUT and i960 Jx probe adapter, follow these steps:

CAUTION. *Failure to power down your SUT before removing the power from the probe adapter might permanently damage the i960 Jx microprocessor and SUT.*

1. Power down the SUT.
2. Unplug the power supply for the probe adapter from the electrical outlet.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 163 i960 Jx support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the i960 Jx support are Address, Data, Control, Intr, ByteEnbl, Aux, and Misc. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–6.

Clocking Options

The TMS 163 support offers a microprocessor-specific clocking mode for the i960 Jx microprocessor. This clocking mode is the default selection whenever you load the 960JX support.

A description of how cycles are sampled by the module using the TMS 163 support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking option for the TMS 163 application is Alternate Bus Master Cycles. Alternate Bus Master Cycles are acquired when you select Included.

Alternate Bus Master Cycles

An alternate bus master cycle is defined as the cycle in which the i960 Jx microprocessor gives up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Symbols

The TMS 163 support supplies one symbol table file. The 960JX_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file 960JX_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value LOCK* HOLDA WIDTH1 WIDTH0 / DEN* BLAST* W/R* D/C*	Meaning
FETCH	1 0 X X / X X 0 0	Memory code read (Opcode Fetch)
READ	1 0 X X / 0 0 0 1	Non-Burst memory read cycle; also indicates the last cycle in a Burst read access
WRITE	1 0 X X / 0 0 1 1	Non-Burst memory write cycle; also indicates the last cycle in a Burst write access
HALT	X X 1 1 / X X X X	Microprocessor halted
L_READ	0 0 X X / 0 0 0 1	Read cycle of the atomic memory access
L_WRITE	0 0 X X / 0 0 1 1	Write cycle of the atomic memory access
DMA_READ	X 1 X X / X X 0 X	DMA read from memory
DMA−WRITE	X 1 X X / X X 1 X	DMA write to memory
BURST_RD	1 0 X X / 0 1 0 1	Burst read from memeory
BURST_WR	1 0 X X / 0 1 1 1	Burst write to memory
UNDEFINED	X X X X / X X X X	None of the above

The TMS 163 software also supplies several range symbol table files for the Address channel group. The range symbol files replace specific ranges of Address channel group values with symbolic values when the symbolic display is selected for the group.

Table 2–2 shows the name, lower and upper bounds, and meaning for the symbols in the file 960JX_IBR, the Initialization Boot Record symbol table for the Address group.

Table 2–2: IBR symbol table definitions for the Address group

Symbol	Address group value		Meaning
	Lower bound	Upper bound	
IBR_BCON2	FEFF FF38	FEFF FF3B	PMCON14_15, byte 2
IBR_BCON3	FEFF FF3C	FEFF FF3F	PMCON14_15, byte 3
IBR_FSTIP	FEFF FF40	FEFF FF43	First instruction point
IBR_PRCB	FEFF FF44	FEFF FF47	PRCB pointer
IBR_CHK_W	FEFF FF48	FEFF FF5F	Bus confidence self test check words

Table 2–3 shows the name, lower and upper bounds, and meaning for the symbols in the file 960JX_PCRB, the Process Control Block symbol table for the Address group.

Table 2–3: PRCB symbol table definitions for the Address group

Symbol	Address group value		Meaning
	Lower bound	Upper bound	
PRCB_FTB	0	3	Fault table base address
PRCB_CTB	4	7	Control table base address
PRCB_ACR	8	B	AC register initial image
PRCB_FCW	C	F	Fault configuration word
PRCB_ITB	10	13	Interrupt table base address
PRCB_SPB	14	17	System procedure table base address
PRCB_ISP	1C	1F	Interrupt stack pointer
PRCB_ICC	20	23	Instruction cache configuration word
PRCB_RCC	24	27	Register cache configuration word

Table 2–4 shows the name, lower and upper bounds, and meaning for the symbols in the file 960JX_CTBL, the Control Table symbol table for the Address group.

Table 2–4: Control Table symbol table definitions for the Address group

	Address group value		
Symbol	Lower bound	Upper bound	Meaning
IMAP0	10	13	Interrupt Map 0
IMAP1	14	17	Interrupt Map 1
IMAP2	18	1B	Interrupt Map 2
ICON	1C	1F	Interrupt Configuration
PMCON01	20	23	Physical memory region 0:1 Configuration
PMCON23	28	2B	Physical memory region 2:3 Configuration
PMCON45	30	33	Physical memory region 4:5 Configuration
PMCON67	38	3B	Physical memory region 6:7 Configuration
PMCON88	40	43	Physical memory region 8:9 Configuration
PMCON1011	48	4B	Physical memory region 10:11 Configuration
PMCON1213	50	53	Physical memory region 12:13 Configuration
PMCON1415	58	5B	Physical memory region 14:15 Configuration
TC	68	6B	Trace Controls
BCON	6C	6F	Bus configuration word

Table 2–5 shows the name, lower and upper bounds, and meaning for the symbols in the file 960JX_INT, the Interrupt Table symbol table for the Address group.

Table 2–5: INT symbol table definitions for the Address group

	Address group value		
Symbol	Lower bound	Upper bound	Meaning
PEND_PRI	0	3	Pending priority
PEND_INT	4	23	Pending interrupts
INT_VECT	24	403	Vector entry

Table 2–6 shows the name, lower and upper bounds, and meaning for the symbols in the file 960JX_FAULT, the Fault Table symbol table for the Address group.

Table 2–6: FAULT symbol table definitions for the Address group

	Address group value		
Symbol	**Lower bound**	**Upper bound**	**Meaning**
PAR_FAULT	0	7	Overide/Parallel Fault
TR_FAULT	8	F	Trace Fault
OP_FAULT	10	17	Operation Fault
AR_FAULT	18	1F	Arithmetic Fault
CON_FAULT	28	2F	Constraint Fault
PRO_FAULT	38	3F	Protection Fault
TYP_FAULT	50	5F	Type Fault

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- Changing the way data is displayed
- Changing disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 960JX support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE*. Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–10.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–7 shows these special characters and strings, and gives a definition of what they represent.

Table 2–7: Meaning of special characters in the display

Character or string displayed	Meaning
>> or m	The instruction was manually marked as a program fetch
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.

Hardware Display Format

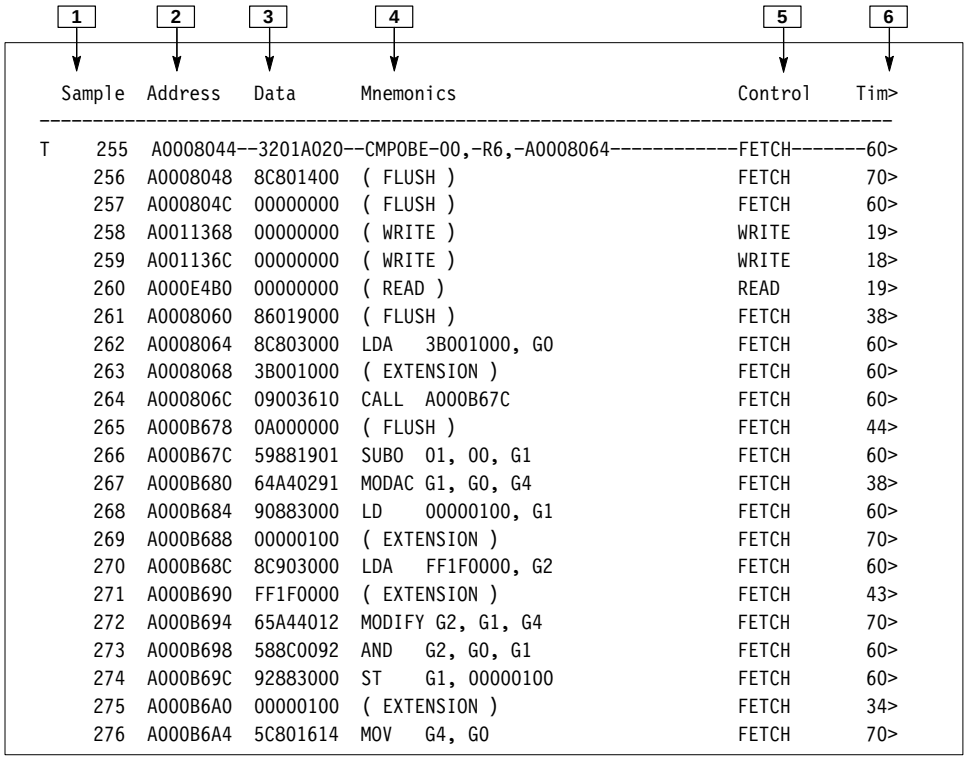
In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–8 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–8: Cycle type definitions

Cycle type	Definition
(READ)	Basic read from memory
(WRITE)	Basic write to memory
(BURST_READ)	Burst read from memory
(BURST_WRITE)	Burst write to memory
(LOCKED_READ)	Read cycle of an atomic memory access
(LOCKED_WRITE)	Write cycle of an atomic memory access
(DMA_READ)	DMA read from memory
(DMA_WRITE)	DMA write to memory
(HALT)	Processor halt
(STEST FAIL)	Processor has failed in self test
(RESET LOCATION)	Processor reset and started fetching at address FEFF FF38
(FLUSH)*	Instruction fetch not executed by the processor
(EXTENSION)†	The second word of an extended opcode fetched from memory
(PREFETCH BYTE)†	8-bit instruction fetch
(PREFETCH HALF-WORD)†	16-bit instruction fetch
* ILLEGAL INSTRUC-TION *†	Not a valid instruction
(UNKNOWN)	Unrecognized cycle type

* **Computed cycle types.**

Figure 2–1 shows an example of the Hardware display.




```
  Sample  Address   Data      Mnemonics                                Control    Tim>
-------------------------------------------------------------------------------------
T    255  A0008044--3201A020--CMPOBE-00,-R6,-A0008064------------FETCH-------60>
     256  A0008048  8C801400  ( FLUSH )                            FETCH       70>
     257  A000804C  00000000  ( FLUSH )                            FETCH       60>
     258  A0011368  00000000  ( WRITE )                            WRITE       19>
     259  A001136C  00000000  ( WRITE )                            WRITE       18>
     260  A000E4B0  00000000  ( READ )                             READ        19>
     261  A0008060  86019000  ( FLUSH )                            FETCH       38>
     262  A0008064  8C803000  LDA   3B001000, G0                   FETCH       60>
     263  A0008068  3B001000  ( EXTENSION )                        FETCH       60>
     264  A000806C  09003610  CALL  A000B67C                       FETCH       60>
     265  A000B678  0A000000  ( FLUSH )                            FETCH       44>
     266  A000B67C  59881901  SUBO  01, 00, G1                     FETCH       60>
     267  A000B680  64A40291  MODAC G1, G0, G4                   FETCH       38>
     268  A000B684  90883000  LD    00000100, G1                FETCH       60>
     269  A000B688  00000100  ( EXTENSION )                      FETCH       70>
     270  A000B68C  8C903000  LDA   FF1F0000, G2                 FETCH       60>
     271  A000B690  FF1F0000  ( EXTENSION )                      FETCH       43>
     272  A000B694  65A44012  MODIFY G2, G1, G4                  FETCH       70>
     273  A000B698  588C0092  AND   G2, G0, G1                   FETCH       60>
     274  A000B69C  92883000  ST    G1, 00000100                FETCH       60>
     275  A000B6A0  00000100  ( EXTENSION )                      FETCH       34>
     276  A000B6A4  5C801614  MOV   G4, G0                       FETCH       70>
```

Figure 2–1: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the i960 Jx address bus.

3 **Data Group.** Lists data from channels connected to the i960 Jx data bus.

4 **Mnemonics Column.** Lists the disassembled instructions and cycle types.

5 **Control Group.** Lists data from channels connected to i960 Jx microprocessor control signals (shown symbolically).

6 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the i960 Jx microprocessor are as follows:

B	BX	CALLX
BAL	CALL	FMARK
BALX	CALLS	RET

Instructions that might generate a change in the flow of control in the i960 Jx microprocessor are as follows:

BBC	BO	CMPOBE	FAULTL
BBS	CMPIBE	CMPOBG	FAULTLE
BE	CMPIBG	CMPOBGE	FAULTNE
BG	CMPIBGE	CMPOBL	FAULTNO
BGE	CMPIBL	CMPOBLE	FAULTO
BL	CMPIBLE	CMPOBNE	MARK
BLE	CMPIBNE	FAULTE	
BNE	CMPIBNO	FAULTG	
BNO	CMPIBO	FAULTGE	

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the i960 Jx microprocessor are as follows:

CALL	CALLS	CALLX	RET

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the i960 Jx support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

- Specify the starting address of the exception vector table.
- Specify the starting address of the fault vector table.

The i960 Jx microprocessor support product has two additional fields: Interrupt Table Base, and Fault Table Base. These fields appear in the area indicated in the basic operations user manual.

***NOTE**. Do not enter an address that resides in the internal RAM in these fields. Do not enter the same value in both fields. If you enter an address value that resides in the internal RAM, is outside the range, or is the same in both fields, the default value is used. With the default value, interrupts and faults will not be identified.*

Interrupt Table Base. You can specify the starting address of the interrupt table in hexadecimal. The address range is 00000400-FEFFFFFF and the default starting address is 0x00000500.

Fault Table Base. You can specify the starting address of the fault table in hexadecimal. The address range is 00000400-FEFFFFFF and the default starting address is 0x00000600.

***NOTE**. The default values are arbitrary, but should be greater than 3FF.*

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)

You can mark word aligned address sequences, but not the second, third, or fourth bytes in an 8-bit memory region, or the second byte in a 16-bit region. If you mark the word aligned sequence in an 8- or 16-bit region, the same mark is applied to the next three or one bytes, respectively.

When an instruction is missed, two or four words of instructions are fetched and only valid bits corresponding to the fetched words are set in the buffer. No external instruction fetches are generated until there is a “miss” within the buffer, even in the presence of forward and backward branches.

If the target of the branch is not double word aligned, the word previous to the target will also be fetched but not executed. You can use the Mark Cycles function to correct disassembled data.

Mark selections are as follows:

```
Opcode
Extension
Flush

Undo mark
```

Information on basic operations contains more details on marking cycles.

Displaying Exception Vectors

The disassembler can display exception vectors (interrupts and faults). The interrupt and fault tables must reside in external memory for the accesses to be visible on the bus and to the disassembler.

You can relocate the interrupt table by entering the starting address in the Interrupt Table Base field. The Interrupt Table Base field provides the disassembler with the base address; enter an eight-digit hexadecimal value corresponding to the base of the base address of the interrupt table.

You can relocate the fault table by entering the starting address in the Fault Table Base field. The Fault Table Base field provides the disassembler with the base address; enter an eight-digit hexadecimal value corresponding to the base address of the fault table.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Table 2–9 lists i960 Jx exception vectors.

Table 2–9: Exception vectors

Exception number	Location in IV* table (in hexadecimal)	Displayed exception name
8	024	(INT 8 VECTOR)
9	028	(INT 9 VECTOR)
10	02C	(INT 10 VECTOR)
...	...	...
243	3D0	(INT 243 VECTOR)
244-247	3D4-3E0	(RESERVED)
248	3E4	(NMI PROCEDURE)
249-251	3E8-3F0	(RESERVED)
252	3F4	(INT 252 VECTOR)
253	3F8	(INT 253 VECTOR)
254	3FC	(INT 254 VECTOR)
255	400	(INT 255 VECTOR)

*** IV means interrupt vector.**

Table 2–10 lists i960 Jx fault vectors.

Table 2–10: Fault vectors

Fault number	Location in Fault table (in hexadecimal)	Displayed fault name
0	00	(OVERRIDE/P'LL FAULT)
1	08	(TRACE FAULT)
2	10	(OPERATION FAULT)
3	18	(ARITHMETIC FAULT)
4	20	(RESERVED)
5	28	(CONSTRAINT FAULT)
6	30	(RESERVED)
7	38	(PROTECTION FAULT)
8-9	40	(RESERVED)
Ah	50	(TYPE FAULT)
Bh-Fh	58	(RESERVED)

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your i960 Jx microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires i960 Jx signals
- List of other accessible microprocessor signals and extra probe channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a i960 Jx microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

Circuitry on the probe adapter can be powered from either the SUT or an external power source. Refer to *Applying and Removing Power* in the *Getting Started* chapter on page 1–12 for information on using an external power source.

The probe adapter accommodates the Intel i960 Jx microprocessor in a 132-pin PGA package. The probe adapter with the optional PGA-to-QFP converter clip accommodates the Intel i960 Jx microprocessor in a 132-pin PQFP package.

Configuration

There is one jumper on the probe adapter. The Power Source jumper is set to power the probe adapter from the system under test (SUT) or from an alternate power supply.

To power the probe adapter from an alternate power supply, place the jumper on pins 1 and 2. To power the probe adapter from the SUT, place the jumper on pins 2 and 3.

Figure 3–1 shows the Power Source jumper location on the probe adapter.

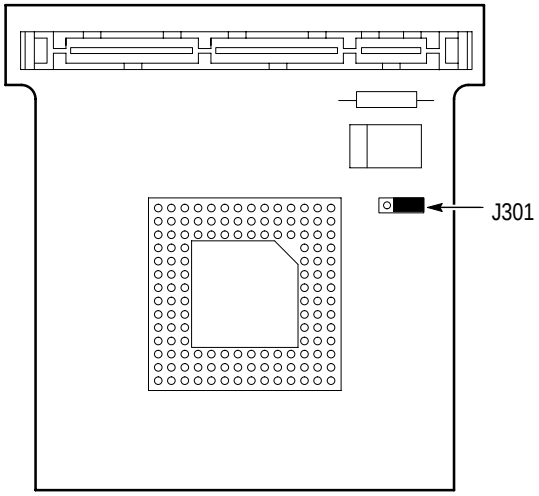


Figure 3–1: Jumper location on the probe adapter

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–1, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements
Adapter DC power requirements	
Voltage	4.75 – 5.25 VDC
Current	I max (calculated) 110 mA
Probe adapter power supply requirements	
Voltage	90-265 VAC
Current	1.1 A maximum at 100 VAC
Frequency	47 – 63 Hz
Power	25 W maximum
SUT clock	
Clock rate	
i960 JA/JF	Max. 33 MHz*

Table 3–1: Electrical specifications (cont.)

Characteristics	Requirements	
i960 JD	Max. 25 MHz*	
Minimum setup time required		
All signals	5 ns	
Minimum hold time required		
All signals	0 ns	
	Specification	
Measured typical SUT signal loading	**AC load**	**DC load**
AD31-A4, A3-A2, D3-D0, BE3-BE0, LOCK*, D/C*, W/R*, WIDTH1-WIDTH0, HOLDA, RDYRCV*, DEN*, ADS*, XINT7*-XINT0*, NMI*, DT/R*, FAIL*, HOLD, RESET*, ALE, BSTAT, TDI, TDO	3.5 pF	74FCT16244
CLKIN, BLAST*	3.5 PF	2 74FCT16244s

*** Tested to 33 MHz.**

Table 3–2 shows the environmental specifications.

Table 3–2: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed i960 Jx microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–3 shows the certifications and compliances that apply to the probe adapter.

Table 3–3: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.

Figure 3–2 shows the dimensions of the probe adapter. The figure also shows the minimum vertical clearance of the high-density probe cable.

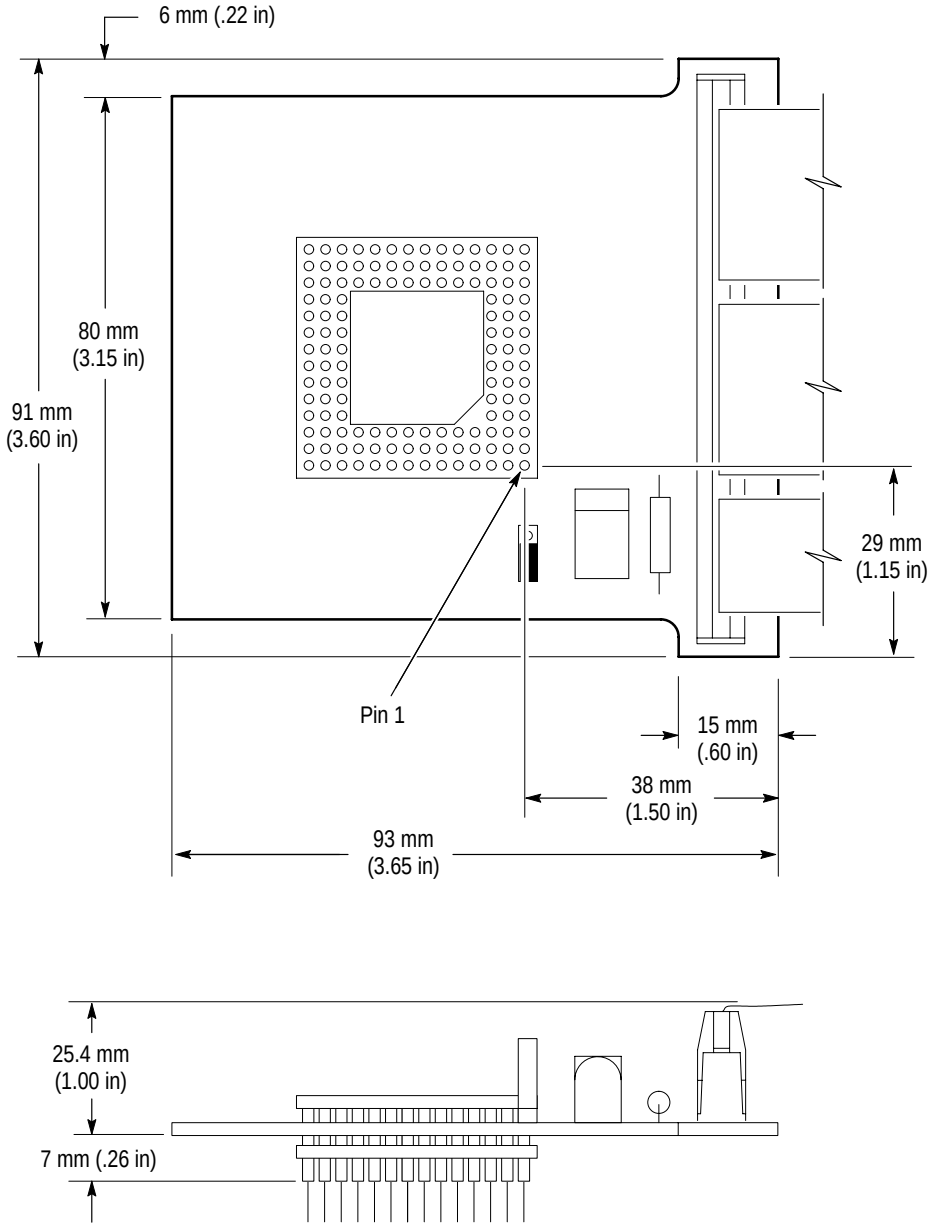


Figure 3–2: Dimensions of the probe adapter

Figure 3–3 shows the dimensions of the PGA-to-QFP converter clip connected to the probe adapter. Figure 3–2 shows the dimensions of the probe adapter.

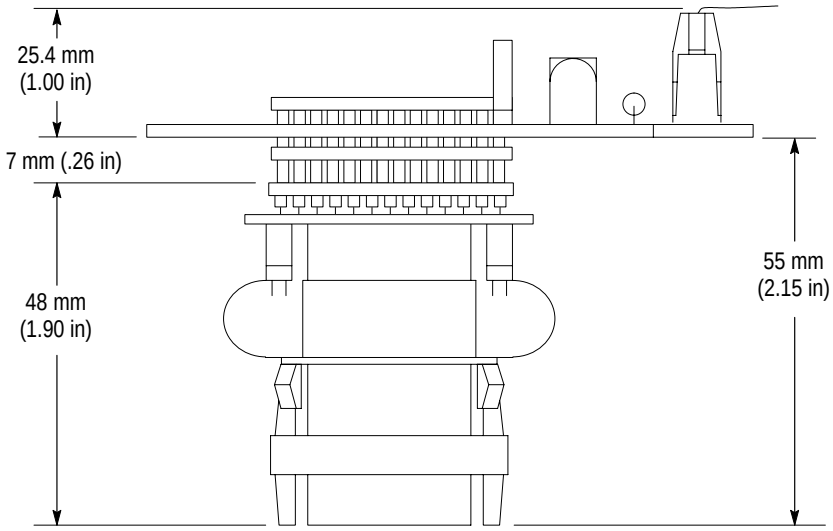


Figure 3–3: Dimensions of the PGA-to-QFP converter clip

Channel Assignments

Channel assignments shown in Table 3–4 through Table 3–11 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- An asterisk (*) a tilde (~) a pound sign (#) following a signal name indicates an active low signal.
- An equals sign (=) following a signal name indicates that it is double probed.

Table 3–4 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–4: Address group channel assignments

Bit order	Section:channel	i960 Jx signal name
31	A3:7	AD31
30	A3:6	AD30
29	A3:5	AD29
28	A3:4	AD28
27	A3:3	AD27
26	A3:2	AD26
25	A3:1	AD25
24	A3:0	AD24
23	A2:7	AD23
22	A2:6	AD22
21	A2:5	AD21
20	A2:4	AD20
19	A2:3	AD19
18	A2:2	AD18
17	A2:1	AD17
16	A2:0	AD16
15	A1:7	AD15
14	A1:6	AD14
13	A1:5	AD13
12	A1:4	AD12
11	A1:3	AD11
10	A1:2	AD10
9	A1:1	AD9
8	A1:0	AD8
7	A0:7	AD7
6	A0:6	AD6
5	A0:5	AD5
4	A0:4	AD4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1†
0	A0:0	A0†

† **Connected to ground.**

Table 3–5 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

NOTE. *Since the microprocessor multiplexes address A31-A4 and data D31-D4 (as the AD31-AD4 signals), the D3:7-0, D2:7-0, D1:7-0 and D0:7-4 channel probes do not need to be connected.*

These channels are not considered to be extra channels, even though they are not connected. Do not use them to make connections to other signals in your SUT.

Table 3–5: Data group channel assignments

Bit order	Section:channel	i960 Jx signal name
31	D3:7	AD31
30	D3:6	AD30
29	D3:5	AD29
28	D3:4	AD28
27	D3:3	AD27
26	D3:2	AD26
25	D3:1	AD25
24	D3:0	AD24
23	D2:7	AD23
22	D2:6	AD22
21	D2:5	AD21
20	D2:4	AD20
19	D2:3	AD19
18	D2:2	AD18
17	D2:1	AD17
16	D2:0	AD16
15	D1:7	AD15
14	D1:6	AD14
13	D1:5	AD13
12	D1:4	AD12
11	D1:3	AD11
10	D1:2	AD10
9	D1:1	AD9
8	D1:0	AD8
7	D0:7	AD7
6	D0:6	AD6

Table 3–5: Data group channel assignments (cont.)

Bit order	Section:channel	i960 Jx signal name
5	D0:5	AD5
4	D0:4	AD4
3	D0:3†	AD3
2	D0:2†	AD2
1	D0:1†	AD1
0	D0:0†	AD0

† These channels must be connected.

Table 3–6 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–6: TMS 163 Control group channel assignments

Bit order	Section:channel	i960 Jx signal name
7	C2:7	LOCK*
6	C2:3	HOLDA
5	C3:0	WIDTH1
4	C2:4	WIDTH0
3	C2:1	DEN*
2	C2:5	BLAST*
1	C3:4	W/R*
0	C2:6	D/C*

Table 3–7 shows the acquisition probe section and channel assignments for the ByteEnbl group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–7: TMS 163 ByteEnbl group channel assignments

Bit order	Section:channel	i960 Jx signal name
3	C3:6	BE3*
2	C3:2	BE2*
1	C3:5	BE1*
0	C3:1	BE0*

Table 3–8 shows the acquisition probe section and channel assignments for the Aux group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–8: TMS 163 Aux group channel assignments

Bit order	Section:channel	i960 Jx signal name
1	C2:2	RDYRCV*
0	C2:0	ADS*

Table 3–9 shows the acquisition probe section and channel assignments for the Intr group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–9: TMS 163 Intr group channel assignments

Bit order	Section: channel	i960 Jx signal name
8	C0:5	NMI*‡
7	C1:7	XINT7*‡
6	C1:3	XINT6*‡
5	C0:7	XINT5*‡
4	C0:3	XINT4*‡
3	C1:6	XINT3*‡
2	C1:2	XINT2*‡
1	C0:6	XINT1*‡
0	C0:2	XINT0*‡

‡ **Signal not required for disassembly.**

Table 3–10 shows the acquisition probe section and channel assignments for the Misc group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–10: TMS 163 Misc group channel assignments

Bit order	Section: channel	i960 Jx signal name
8	C1:5	ALE‡
7	C0:1	HOLD‡
6	C1:1	DT/R*‡

Table 3–10: TMS 163 Misc group channel assignments (cont.)

Bit order	Section: channel	i960 Jx signal name
5	C1:0	FAIL*‡
4	C3:3	RESET*‡
3	C3:7	CLKIN‡
2	C1:4	BSTAT‡
1	C0:4	TDI‡
0	C0:0	TDO‡

‡ **Signal not required for disassembly.**

Table 3–11 shows the probe section and channel assignments for the clock probes (not part of any group) and the i960 Jx signal to which each channel connects.

Table 3–11: Clock channel assignments

Section:channel	i960 Jx signal name
CK:1	BLAST*=
CK:0	CLKIN=

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–11, you must connect another channel probe to the signal, a technique called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

How Data is Acquired

This part of this chapter explains how the module acquires i960 Jx signals using the TMS 163 software and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra probe channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the 960JX support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the i960 Jx bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–4 shows the sample points and the master sample points.

The CSM has two states: Address_Ta and Data_Td. The CSM uses these two states to handle the address (Ta), wait/data (Tw/Td), recovery (Tr), and hold (Th) states of the i960 Jx microprocessor.

Sampling occurs on the rising edge of the CLKIN signal.

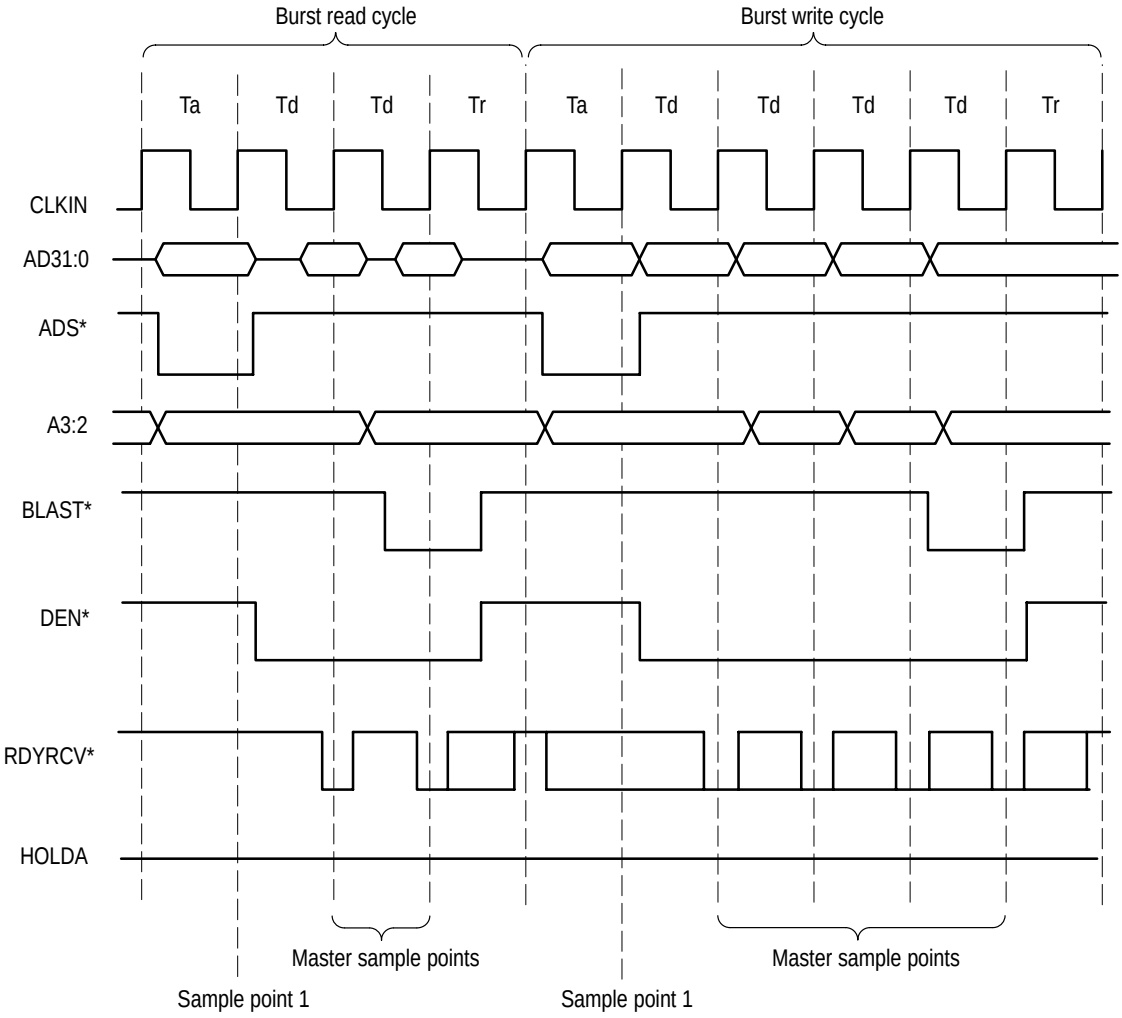


Figure 3–4: i960 Jx bus timing

The CSM enters the Data_Td state from the Address_Ta state only if the ADS* signal is asserted, and the HOLDA signal is not asserted when DMA cycles are excluded or asserted when DMA cycles are included.

In the Address_Ta state, the ADDR31-ADDR4, W/R*, ADS*, ALE, CLKIN, RESET*, LOCK*, HOLDA, WIDTH1, WIDTH0, NMI*, XINT7*-XINT0*, HOLD, and FAIL* signals are sampled on the assertion of the ADS* signal.

In the Data_Td state, the D31-D0, A3-A0, BE3*-BE0*, D/C*, BLAST*, DEN*, and RDYRCV* signals are sampled when the DEN* and RDYRCV* signals are asserted. If it is the last data transfer of the burst and nonburst accesses, the BLAST* signal is asserted which takes the CSM to the address state. If BLAST* is not asserted, the CSM waits in the data state, which indicates the burst access. In these three cases, the HOLDA signal is not asserted.

If the RDYRCV* signal is not asserted, the CSM waits in the data state without strobing any of the address, data, or control signals. This means that the i960 Jx microprocessor is in the wait state (Tw). When DMA cycles are included and the HOLDA and DEN* signals are asserted, it is a DMA access. The CSM goes to the Address_Ta state, data and control signals are sampled, and the master sample is logged. If DEN*, BLAST*, and ADS* signals are not asserted, the CSM comes back to the Address_Ta state without logging a master sample.

The microprocessor always has a recovery state (Tr) state following the Tw/Td state. This allows the system components adequate time to remove their outputs from the bus before the microprocessor drives the next address on the multiplexed address/data signals. But the CSM goes to the Address_Ta state after the last transfer of the bus access. It remains in the same state until the bus recovers, and the BLAST* signal and others are inactive. When the recovery state completes, if no new accesses are required, the bus enters the Ti (idle state). The CSM waits in the Address_Ta state without logging in any samples.

Clocking Options

The clocking algorithm for the i960 Jx microprocessor support has two variations: Alternate Bus Master Cycles Excluded, and Alternate Bus Master Cycles Included.

Alternate Bus Master Cycles Excluded. Whenever the HOLDA signal is high, no bus cycles are logged in. Only bus cycles initiated by the i960 Jx microprocessor (HOLDA low) will be logged in.

Alternate Bus Master Cycles Included. All bus cycles, including Alternate Bus Master cycles and Backoff cycles, are logged in.

When the HOLDA signal is high, the i960 Jx microprocessor has given up the bus to an alternate device. The design of the i960 Jx system affects what data will be logged in. The module samples the data at the pins of the i960 Jx microprocessor. To properly log in bus activity, any buffers between the i960 Jx microprocessor and the alternate bus master must be enabled and pointing at the i960 Jx microprocessor.

There are three possible i960 Jx system designs and clocking interactions when an alternate bus master has control of the bus. The three different possibilities are listed below (in each case, the HOLDA signal is logged in as a high level).

- If the alternate bus master drives the same control lines as the i960 Jx microprocessor, and the i960 Jx microprocessor sees these signals, the bus activity is logged in like normal bus cycles except that the HOLDA signal is high.
- If none of the control lines are driven or if the i960 Jx microprocessor can not see them, the module will still clock in an alternate bus master cycle. The information on the bus, one clock prior to the HOLDA signal going low, is logged in. If the ADS# signal goes low on the same clock when the HOLDA signal goes low, the address that gets logged in will be the next address, not the address that occurred one clock before the HOLDA signal went low.
- If some of the i960 Jx microprocessor control lines are visible (but not all), the module logs in what it determines is valid from the control signals and logs in the remaining bus signals one clock cycle prior to the HOLDA signal going low. If the ADS# signal goes low on the same clock that the HOLDA signal goes low, the next address will be logged in instead of the previously saved address.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so that you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–6. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals On the Probe Adapter

The LAHDP2 probe contains pins for the C0 and C1 channel probes, you can connect the probes from the 92A96 module to pins on the LAHDP2 probe, because the i960 Jx signals can be useful for general purpose analysis. Since the signals are not required for disassembly, you do not have to connect the probes.

Table 3–12 shows the microprocessor signals available if you connect the C0 and C1 probes of the 92A96 module to the LAHDP2 probe. The signals are already assigned to either the Intr or Misc channel groups.

Table 3–12: i960 Jx signals available on C0 and C1 (92A96 only)

C0 channel*	Signal name	C1 channel*	Signal name
7	XINT5*	7	XINT7*
6	XINT1*	6	XINT3*
5	NMI*	5	ALE
4	TDI	4	BSTAT
3	XINT4*	3	XINT6*
2	XINT0*	2	XINT2*
1	HOLD	1	DT/R*
0	TDO	0	FAIL*

*** Sections not available with the 32GPX module.**

Signals Not On the Probe Adapter

The probe adapter does not provide access for the following microprocessor signals:

- STEST
- TCK
- TRST*
- TMS

Extra Channels

Table 3–13 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Table 3–13: Extra module sections and channels

Module	Section: channels
102-channels	Qual:1, Qual:0
136-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0, E3:7-0, E2:7-0, E1:7-0, E0:7-0, Qual:3-0
96-channels	None

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This chapter contains information on the following topics:

- Probe adapter circuit description
- How to replace a fuse

Probe Adapter Circuit Description

The i960 Jx probe adapter does not contain any active circuitry.

Replacing the Fuse

If the fuse on the i960 Jx probe adapter opens (burns out), you can replace it with a 5 A, 125 V fuse. Figure 4–1 shows the location of the fuse on the probe adapter.

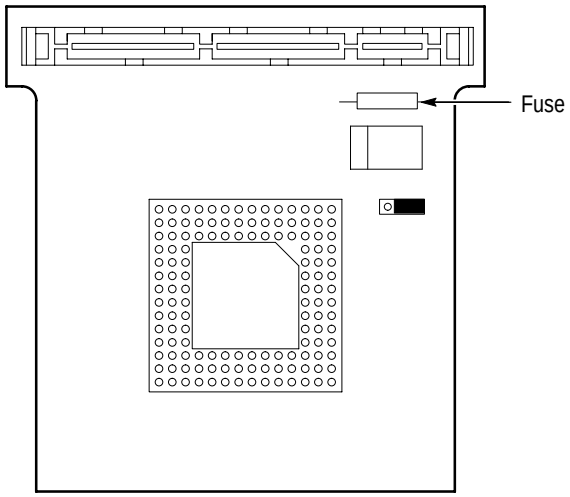


Figure 4–1: Location of the fuse

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 163 i960 Jx microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

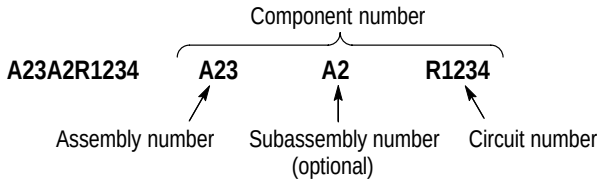
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG, MD 20879
26742	METHODE ELECTRONICS INC	BACKPLAIN DIVISION 7444 WEST WILSON AVE	CHICAGO, IL 60656–4548
61857	SAN–O INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK, NY 11741
63058	MCKENZIE TECHNOLOGY	910 PAGE AVE	FREMONT, CA 945387340
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	010–0597–00			PROBE ADAPTER:80960JX,PGA–132,SOCKETED,TMS 163	80009	010–0597–00
A01	136–0940–00			SOCKET,PGA::PCB,132 POS,14 X 14,0.1 CTR,0.170 H X 0.170 TAIL,OPEN CTR,SYMMETRICAL,PAT 1415	63058	PGA 132H101B1–1414F
A01	174–3418–00			CA ASSY,RF:TLC,MICRO–STRIP,TLC,50 OHM,FEP,PROP DELAY 1.4NS,12.0 L,100 POS,PLUG,LATCHING BOT	00779	1–340014–0
A01	671–3800–00			CIRCUIT BR ASSY:80960JX,PGA–132, SOCKETED,389–2212–00 WIRED	80009	671–3800–00
A01F401	159–0059–00			FUSE,WIRE LEAD:5A,125V	61857	SPI–5A
A01J301	131–4530–00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION	00779	104344–1
A01J401	131–5527–00			JACK,POWER DC:PCB,MALE,RTANG,2MM PIN,11MM H(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWI	0LXM2	DJ005A
A01J501	131–5947–00			CONN,BOX:PCB,MICRO–STRIP,FEMALE,STR,100 POS,0.05 CTR,W/GRD PLANE,0.320 H X 0.125 TAIL,LAT	00779	121289–7
A01P301	131–4356–00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER	26742	9618–302–50

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 163 i960 Jx microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG, MD 20879
26742	METHODE ELECTRONICS INC	BACKPLAIN DIVISION 7444 WEST WILSON AVE	CHICAGO, IL 60656–4548
61857	SAN–O INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK, NY 11741
63058	MCKENZIE TECHNOLOGY	910 PAGE AVE	FREMONT, CA 945387340
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0597–00			1	PROBE ADAPTER:80960JX,PGA–132,SOCKETED	80009	010–0597–00
–1	174–3418–00			1	CA ASSY,RF:TLC,MICRO–STRIP,TLC,50 OHM,FEP,PROP DELAY 1.4NS,12.0 L,100 POS,PLUG,LATCHING BOT	00779	1–340014–0
–2	131–4356–00			1	CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER	26742	9618–302–50
–3	131–4530–00			1	CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION	00779	104344–1
–4	131–5527–00			1	JACK,POWER DC:PCB,MALE,RTANG,2MM PIN,11MM H(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWI	0LXM2	DJ005A
–5	671–3800–00			1	CIRCUIT BR ASSY:80960JX,PGA–132, SOCKETED,389–2212–00 WIRED	80009	671–3800–00
–6	136–0940–00			2	SOCKET,PGA::PCB,132 POS,14 X 14,0.1 CTR,0.170 H X 0.170 TAIL,OPEN CTR,SYMMETRICAL,PAT 1415	63058	PGA 132H101B1–1414F
–7	103–0406–00			1	CONN, ADAPTER,; QFP, 132–PIN JEDEC TEST CLIP TO PGA SOCKET		
–8	131–5947–00			1	CONN,BOX:PCB,MICRO–STRIP,FEMALE,STR,100 POS,0.05 CTR,W/GRD PLANE,0.320 H X 0.125 TAIL,LAT	00779	121289–7
–9	159–0059–00			1	FUSE,WIRE LEAD:5A,125V	61857	SPI–5A
					STANDARD ACCESSORIES		
	070–9817–00			1	MANUAL,TECH:INSTRUCTION,960JX,DISSASEMBLER, TMS 163	80009	070–9817–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
	119–5061–01			1	POWER SUPPLY:25W,5V 5A,CONCENTRIC 2MM,90–265V,47–63HZ (NOT SHOWN)	14310	SW106KA002F01
	161–0104–00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,98 INCH, RTANG,IEC320,RCPT X STR,NEMA 15–5P,W/CORD GRIP	S3109	ORDER BY DESCRIPTION
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00
	161–0104–06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, EUROPEAN,SAFETY CONTROLLED (OPT A1)	S3109	ORDER BY DESCRIPTION
	161–0104–07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10AMP,2.5 METER, RTANG,IEC320,RCPT X 13A, FUSED, UK PLUG, (13A FUSE), UNITED KINGDOM,SAFETY CONTROL (OPT A2)	S3109	ORDER BY DESCRIPTION
	161–0104–05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, AUSTRALIA,SAFETY CONTROLLED (OPT A3)	S3109	ORDER BY DESCRIPTION
	161–0167–00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, SWISS,NO CORD GRIP, SAFETY CONTROLLED (OPT A5)	S3109	ORDER BY DESCRIPTION

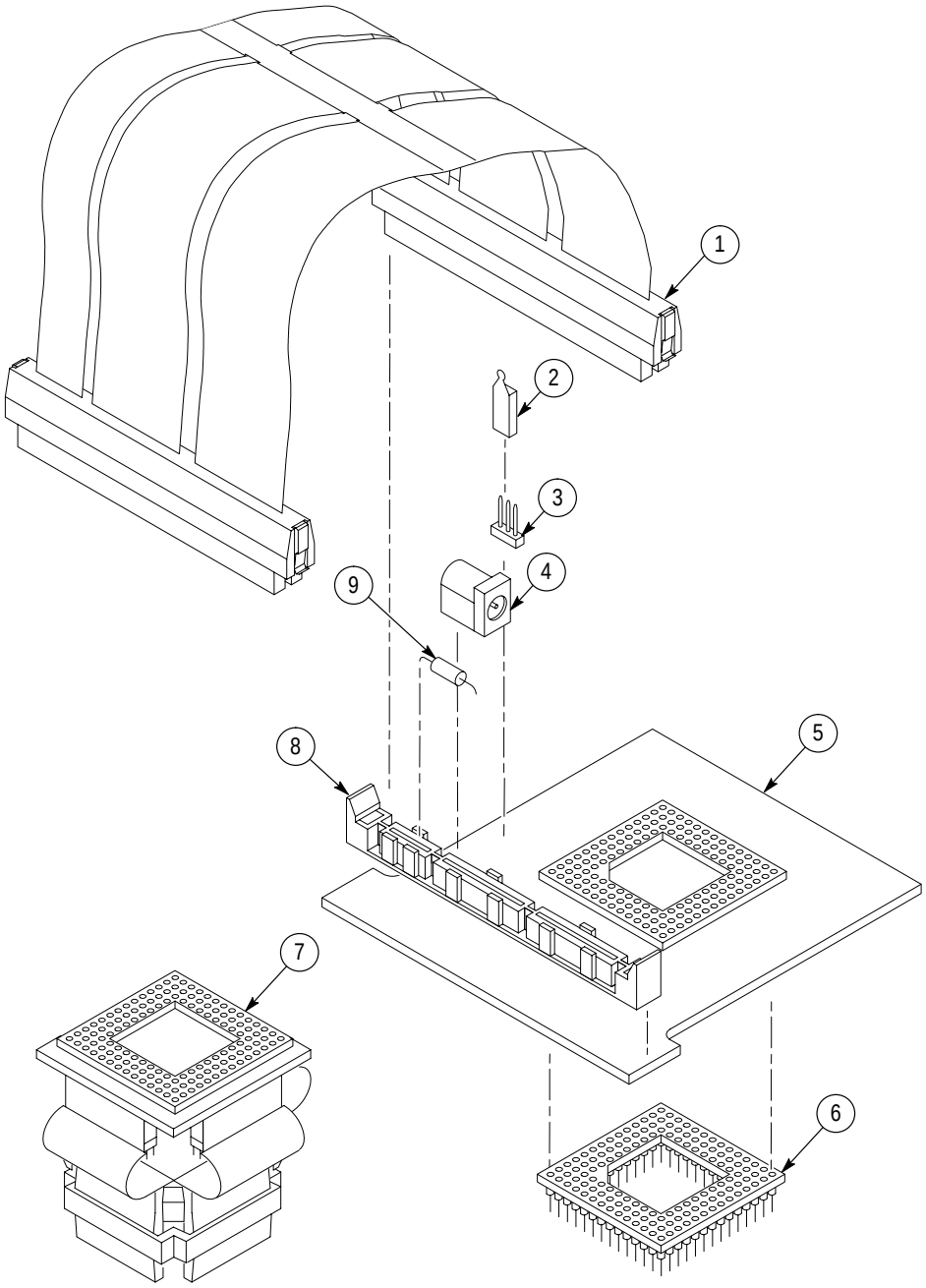


Figure 1: i960 Jx probe adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
2–0	010– 0582–00			1	ADAPTER,PROBE:192–CHANNEL,HIGH DENSITY PROBE	80009	010058200
–1	380–1095–00			1	HOUSING,HALF:UPPER,192 CHANNEL HIGH DENSITY PROBE	80009	380109500
–2	211–0152–00			4	SCR,ASSEM WSHR:4–40 X 0.625,PNH,BRS,NP,POZ	TK0435	ORDER BY DESC
–3	131–5947–00			2	CONN BOX:CPCB, MICRO–STRIP;FEMALE,STR,100 POS,0.05 CTR,W/GRD PLANE,0.320 H X 0.124 TAIL, LATCHING, 4 ROW, 0.05 PCB, STAGGER (J150, J250)	80009	131594700
–4	671–3395–00			1	CKT BD ASSY:192–CHANNELS,HIGH DENSITY PROBE	80009	671339500
–5	380–1096–00			1	HOUSING,HALF:LOWER,192 CHANNEL HIGH DENSITY PROBE	80009	380109600
–6	348–0070–01			2	PAD,CUSHIONING:2.03 X 0.69 X 0.18 SI RBR	85471	ORDER BY DESC
–7	131–4917–00			8	CONN,HDR CPCB,;MALE,STR,1 X 2,0.1 CTR,0.235 MLF X 0.110 TAIL,20 BOLD, TUBE, HIGH TEMP (J300,J340J400,J440J500,J640,J600)	53387	131491700
–8	131–5267–00			5	CONN,HDR CPCB,;MALE,STR,2 X 40.O.1 CTR,0.234 MLG X 0.110 TAIL, 30 GOLD (J310,J320,J330,J340,J350,J360,J370,J410,J420,J430,J450,J460,J470,J510,J520,J530,J550,J560,J570,J610,J620,J630,J650,J660,J670)	53387	131526700

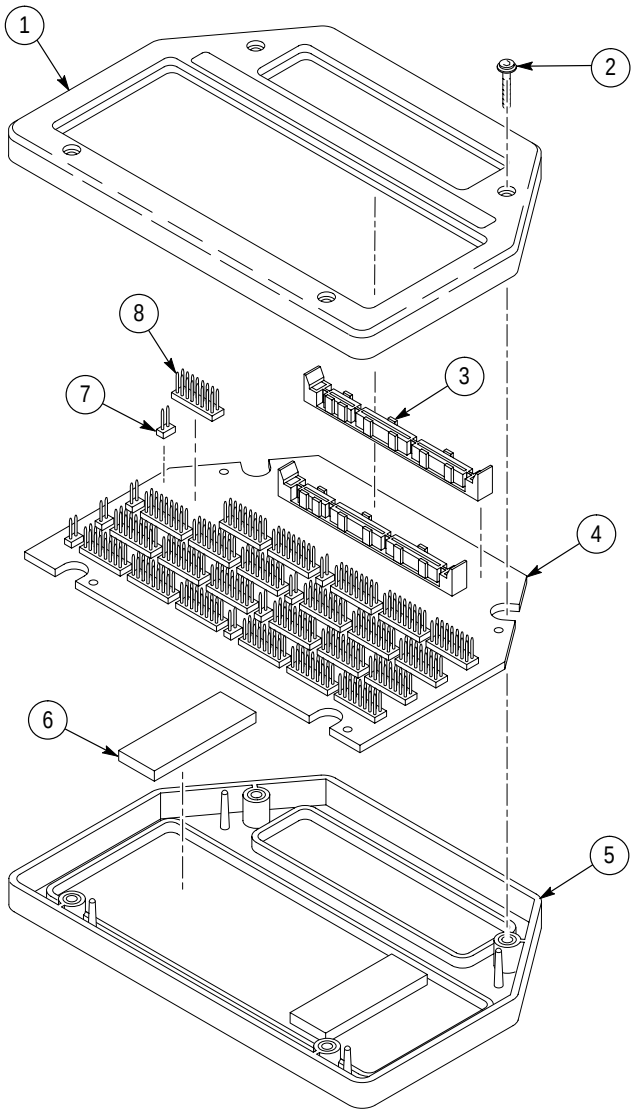


Figure 2: 192-Channel High-Density Probe exploded view

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